Hilroy

80 Pages
27.6 cm x 21.2 cm

Ruled 7 mm • Ligné 7 mm

EXERCISE BOOK
CAHIER D'EXERCICES

NAME/NOM _____

SUBJECT/SUJET CPEN 311

ASSEMBLED IN CANADA WITH IMPORTED MATERIALS
ASSEMBLÉ AU CANADA AVEC DES MATIÈRES IMPORTÉES

12107

Lecture 1

LEC
1/9/20

FPGA (Field Programmable gate array)

PROS:	Cons:
• Can be updated in real time	• Slower
• good for small scale	• Not as good for large-scale

Summary:
① ASIC vs. FPGA
② Look up tables
③ Design process (simulation to synthesis)

Lecture 2

LEC
1/13/20

Two types of writing HDL:
① Behavioural → Higher level, describes logic
② Structural → Low Level, what gate connects to what

System Verilog Syntax and Rules:

```
module flopr (input logic clk, input logic [3:0] d, output logic y);
```

Synchronous Reset → Reset occurs on rising edge of clk
Asynchronous Reset → Resets regardless of where clk is

Lecture 3

LEC
1/16/20

Clicker Quiz

0101
1110

1011
0100

*Use dot convention when connecting ports

Up to SS 93

LEC
1/20/20

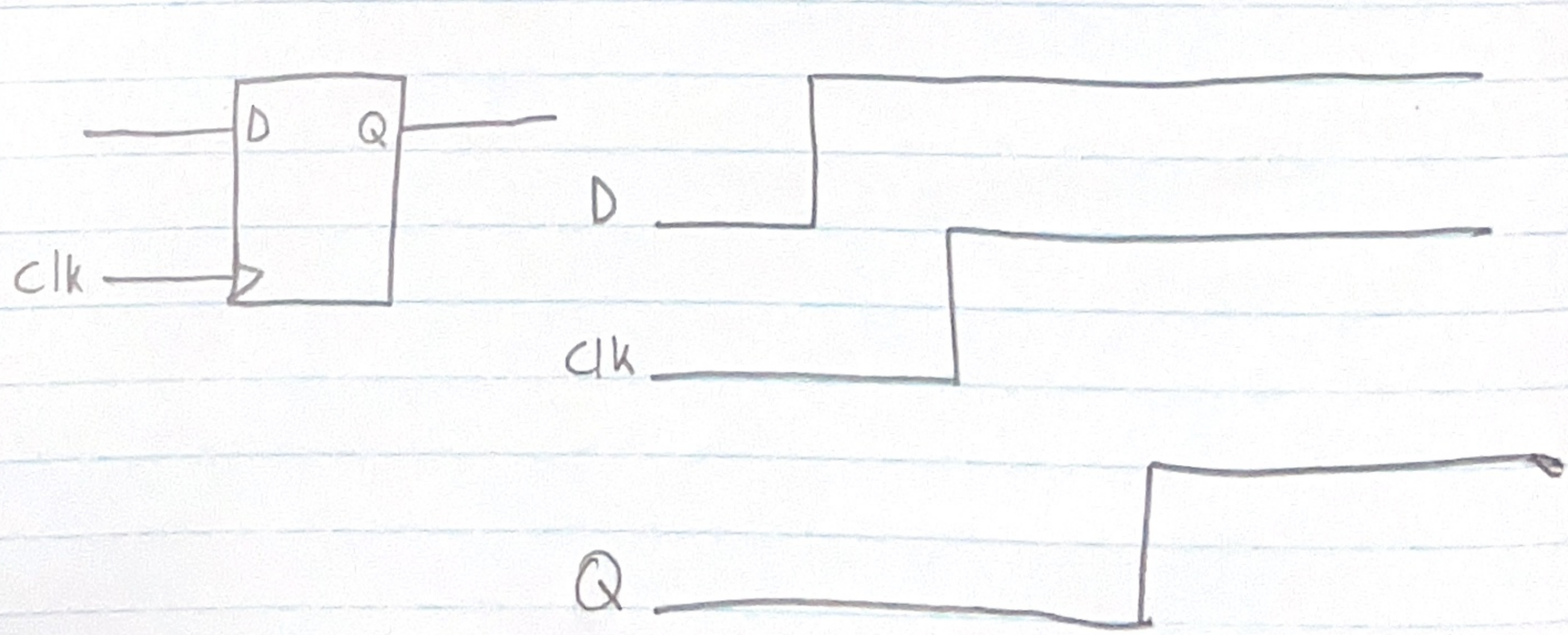
Lecture 4

(Slide Set 3a Circuit timing basics)

Delay — Gate delay
Delay — Path delay

(minimum clock time) ≥ (critical path time) — of all paths circuit wide

Flip Flop delays: (Non-Ideal)



Requirement:

$$t_{clk} \geq t_{clk\text{-}to\text{-}qmax} + t_{critical\text{-}path} + t_{setup}$$

EC
30/20

Lecture 5

EC
10/20

Lecture 8

PicoBlaze → Lab 3 (Easiest Lab?)
Start early → Lab 4 (Most difficult lab)

Store/Fetch → used for scratchpad RAM

Roozbeh → knows where the De2's are

CHV (4 chapters on PicoBlaze)

In-class-activity on PicoBlaze relevant to Lab 3

Lecture 9
(Pipelining)

2/24/20

Laundry example:

Time = $60 + 20(k-1)$ minutes

load 1 ↓ all other loads ↓

$T = (40 + 20k)$ minutes

Latency → When I put something into the system, how long before it is output

Latency ≠ Throughput

↳ Generally more important

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* [Final Exam] → In-Class activity on Pipelining

LEC
3/09/20

Lecture 12

① How to move data from Fast → Slow clk

② Moving data from Slow → Fast clk

[SS13 pg 63] Phase locked Loop → Clk multiplier